The e-Hardware Verification Language (Information Technology: Transmission, Processing & Storage)

Sasan Iman, Sunita Joshi

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I am glad to see this new book on the e language and on verification. I am especially glad to see a description of the e Reuse Methodology (eRM). The main goal of verification is, after all, finding more bugs quicker using given resources, and verification reuse (module-to-system, old-system-to-new-system etc.) is a key enabling component. This book offers a fresh approach in teaching the e hardware verification language within the context of coverage driven verification methodology. I hope it will help the reader und- stand the many important and interesting topics surrounding hardware verification. Yoav Hollander Founder and CTO, Verisity Inc. Preface This book provides a detailed coverage of the e hardware verification language (HVL), state of the art verification methodologies, and the use of e HVL as a facilitating verification tool in implementing a state of the art verification environment. It includes comprehensive descriptions of the new concepts introduced by the e language, e language syntax, and its as- ciated semantics. This book also describes the architectural views and requirements of verifi- tion environments (randomly generated environments, coverage driven verification environments, etc.), verification blocks in the architectural views (i. e. generators, initiators, c- lectors, checkers, monitors, coverage definitions, etc.) and their implementations using the e HVL. Moreover, the e Reuse Methodology (eRM), the motivation for defining such a gui- line, and step-by-step instructions for building an eRM compliant e Verification Component (eVC) are also discussed.

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